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6	BRS	L50	155	(semiconductor same (order or purchase$3)) and (semiconductor same design$3) and ((purcha$3 or order$3) same Intranet or Internet) and (circuit adj design)
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S Magoshi, H Niiyama, S Sato, Y Kato, Y Watanabe, ... - Jpn. J. Appl. Phys, 1999 - jjap.ipap.jp
... **Shunko Magoshi**, Hiromi Niiyama, Shinji Sato, Yoshimitsu Kato, Yumi Watanabe, Tohru ...
Fabricating Sub-100-nm Complementary Metal-Oxide-**Semiconductor** Devices using ...
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S Magoshi, K Koyama, O Ikenaga, S Watanabe, T ... - JPN J APPL PHYS PART 1 REGUL PAP SHORT NOTE., 1992 - csa.com
Shunko Magoshi, Kiyomi Koyama, Osamu Ikenaga, Susumu Watanabe, Tamaki Saito, Shinji
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Throughput Enhancement Strategy of Maskless Electron Beam Direct Writing for Logic Device - group of 2 »
R Inanami, S Magoshi, S Kousai, M Hamada, T ... - INTERNATIONAL ELECTRON DEVICES MEETING, 2000 - ieeexplore.ieee.org
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Stress-Induced Voiding Phenomena for an actual CMOS LSI Interconnects
H NAKAZAWA, M MORITA - ieeexplore.ieee.org
... **Semiconductor** Company. ... Ms. Sachiyo Itoh. Mr. **Shunko Magoshi**, and Mr. Masayuki Hatano
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... jp **Advanced Packaging Engineering Depart., **Semiconductor** Company, Toshiba ... in turn,
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SV Nguyen - IBM JOURNAL OF RESEARCH AND DEVELOPMENT, 1999 - research.ibm.com
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Microprocesses and Nanotechnology Conference, 2001 International
31 Oct.-2 Nov. 2001 Page(s):302 - 303
Digital Object Identifier 10.1109/IMNC.2001.984209

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Inanami, R.; Magoshi, S.; Kousai, S.; Hmada, M.; Takayanagi, T.; Sugihara, K.
Kuroda, T.;
Electron Devices Meeting, 2000. IEDM Technical Digest. International
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☐ 4. **Lithography simulator for EB/DUV intra-level mix and match**
Inanami, R.; Nakasugi, T.; Sato, S.; Mimotogi, S.; Tanaka, S.; Sugihara, K.;
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Nanotechnology '99. 1999 International
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Watanabe, T.; Morooka, T.; Mizuno, H.; Magoshi, S.; Shimizu, T.; Mori, S.; Og
T.; Ohmura, M.; Miyano, K.; Yamada, H.; Tomita, H.; Matsushita, D.; Muraoka,
Takayanagi, M.; Ishimaru, K.; Ishiuchi, H.;
VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on
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☐ 2. **14 nm gate length CMOSFETs utilizing low thermal budget process with ⎸**
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Hokazono, A.; Ohuchi, K.; Takayanagi, M.; Watanabe, Y.; Magoshi, S.; Kato, Y
Mori, S.; Oguma, H.; Sasaki, T.; Yoshimura, H.; Miyano, K.; Yasutake, N.; Sut⎸
Fukui, H.; Watanabe, T.; Tamaoki, N.; Toyoshima, Y.; Ishiuchi, H.;
Electron Devices Meeting, 2002. IEDM '02. Digest. International
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Inaba, S.; Okano, K.; Matsuda, S.; Fujiwara, M.; Hokazono, A.; Adachi, K.; Oh⎸
Fukui, H.; Shimizu, T.; Mori, S.; Oguma, H.; Murakoshi, A.; Itani, T.; Iinuma, T.;
Shibata, H.; Taniguchi, S.; Matsushita, T.; Magoshi, S.; Watanabe, Y.; Takayaı
A.; Oyamatsu, H.; Suguro, K.; Katsumata, Y.; Toyoshima, Y.; Ishiuchi, H.;
Electron Devices Meeting, 2001. IEDM Technical Digest. International
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       Lithography With 100-nm Resolution**
       Magoshi, S.; Niiyama, H.; Sato, S.; Kato, Y.; Watanabe, Y.; Shibata, T.; Ito, M.
       Nakasugi, T.; Sugihara, K.; Okumura, K.;
       Microprocesses and Nanotechnology Conference, 1998 International
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       Nakasugi, T.; Magoshi, S.; Sugihara, K.; Saito, S.; Kihara, N.;
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7	BRS	L15	88	(semiconductor same (order$3 or purchas$3)) and ((order$3 or purchas$4) same (network or Internet or Intranet)) and ((Internet or network) same customer$2) and (semiconductor$2 same specification$2) and pattern
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25	BRS	L33	7	(program adj product) and (semiconductor adj device) and (purchase same (network or Intranet))
26	BRS	L34	1	(program adj product) and (semiconductor adj device) and (purchase same (network or Intranet)) and (record$3 same medium)
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28	BRS	L36	360	705/26.ccls. and semiconductors
29	BRS	L37	4	705/26.ccls. and (semiconductors adj design$3)
30	BRS	L38	1	705/26.ccls. and (program adj product) and (semiconductor adj device) and (purchase same (network or Intranet)) and (record$3 same medium)